IN THE SPECIFICATION:

Kindly amend the paragraph beginning at page 3, line 13 as follows.

The first aspect of the present invention is characterized by including an electrode formed on surface of a semiconductor substrate, wherein said electrode includes a barrier layer consisting of amorphous or microcrystal expressed by the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$; M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

Kindly amend the paragraph beginning at page 3, line 23 as follows.

Another aspect of the present invention is characterized by comprising: a lower electrode formed on a semiconductor substrate; a dielectric layer formed on said lower electrode and constructed by ferroelectric or dielectric having high dielectric constant; and an upper electrode formed on said dielectric layer, wherein said lower electrode includes a barrier layer consisting of amorphous or microcrystal expressed by the following: $M1_xM2_{1-x}$ ($0 < x < 1$; M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

Kindly amend the paragraph beginning at page 4, line 8 as follows.

Another aspect of the present invention is characterized by having: a lower electrode formed on a semiconductor substrate; a dielectric layer formed on said lower electrode and constructed by ferroelectric or dielectric having high dielectric constant; and an upper electrode formed on said dielectric layer, wherein said electrode includes a barrier layer consisting of amorphous or microcrystal between said dielectric layer and said upper electrode expressed by

the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$; M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

A3

Kindly amend the paragraph beginning at page 4, line 19 as follows.

Another aspect of the present invention is characterized by including an electrode formed on surface of a semiconductor substrate, wherein said electrode is constructed by amorphous or microcrystal single layer expressed by the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$; M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

Kindly amend the paragraph beginning at page 5, line 1 as follows.

Another aspect of the present invention is characterized by including process forming an electrode formed on surface of a semiconductor substrate and process forming a dielectric film on the upper layer thereof, wherein process forming said electrode includes process forming a barrier layer consisting of amorphous or microcrystal expressed by the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$; M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

Kindly amend the paragraph beginning at page 5, line 10 as follows.

Another aspect of the present invention is characterized by including: process forming a lower electrode on surface of a semiconductor substrate; process forming a dielectric layer consisting of ferroelectric or dielectric having high dielectric constant on said lower electrode; and process forming an upper electrode on said dielectric layer, wherein said process forming the lower electrode includes process forming amorphous or microcrystal expressed by the following

A3 expression so as to form a dielectric capacitor: $M1_xM2_{1-x}$ ($0 < x < 1$; M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

Kindly amend the paragraph beginning at page 5, line 22 as follows.

Another aspect of the present invention is characterized by including: process forming a lower electrode on a semiconductor substrate; process forming a dielectric layer consisting of ferroelectric or dielectric having high dielectric constant on said lower electrode; process forming a barrier layer consisting of amorphous or microcrystal expressed by the following expression on said dielectric layer: $M1_xM2_{1-x}$ ($0 < x < 1$; M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb); and process forming an upper electrode on said barrier layer so as to form a dielectric capacitor.

Kindly amend the paragraph beginning at page 6, line 8 as follows.

Another aspect of the present invention is characterized by including an electrode formed on surface of a semiconductor substrate, wherein said electrode is constructed by amorphous or microcrystal single layer expressed by the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$; M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

Kindly amend the paragraph beginning at page 6, line 15 as follows.

A semiconductor device of the present invention includes a barrier layer consisting of amorphous or microcrystal between an electrode and a dielectric layer expressed by the following expression: $M1_xM2_{1-x}$ ($0 < x < 1$; M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr; M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).

Kindly amend the paragraph beginning at page 8, line 14 as follows.

A4

A semiconductor device of the present invention is characterized by that having an electrode formed on a surface of a semiconductor substrate, wherein said electrode includes an amorphous or microcrystal barrier layer which includes at least an element chosen from a first group of Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V and Cr and at least an element chosen from a second group of Ta, Ti, Zr, Hf, W, Y, Mo and Nb. A barrier effect is kept good with a ternary chemical compound or higher is used as a barrier. Matching grating constant becomes easier, making it possible to form an electrode with an excellent boundary characteristics.

Kindly amend the paragraph beginning at page 9, line 10 as follows.

A5

Further, other than the above listed binary chemical compounds, a barrier layer of either amorphous or microcrystal of ternary chemical compounds or higher composed of at least an element from a first group of Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V and Cr and at least an element from a second group of Ta, Ti, Zr, Hf, W, Y, Mo and Nb, such as IrTiPt for example, is applicable.

Kindly amend the paragraph beginning at page 25, line 10 as follows.

A6

As described above, according to the present invention, a barrier layer consisting of amorphous or microcrystal is included as an electrode being expressed by the following expression:

$M1_xM2_{1-x}$ ($0 < x < 1$;

M1: Au, Pt, Ir, Pd, Os, Re, Rh, Ru, Cu, Co, Fe, Ni, V, Cr;

M2: Ta, Ti, Zr, Hf, W, Y, Mo, Nb).